Remarks and Arguments

Claims 1-11, 13-28 and 30-36 have been presented for examination. Claims 1, 13, 15, 18, 30, 32, 35 and 36 have been amended.

Claims 1-11, 13-28 and 30-36 have been rejected under 35 U.S.C. §103(a) as obvious over U.S. Patent No. 6,397,268 (Cepulis, previously cited) in view of U.S. Patent No 6,542,953 (Porterfield.) The examiner states that Cepulis discloses all of the recited elements except that it does not disclose sending commands to the predetermined bridge ID values. However, the examiner asserts that Porterfield discloses a PCI bus configuration system in which a processor transmits a configuration command that includes device and bus identifiers that are used to identify certain devices on certain buses. The examiner claims it would have been obvious to incorporate the teachings of Porterfield into those of Cepulis in order to configure computer systems that use both hierarchical and flat configurations.

The Cepulis reference has been previously discussed. It relates to a Peripheral Component Interconnect (PCI) bus system. The PCI bus system comprises a set of interconnected busses and each bus has a set of slots into which PCI devices can be plugged. Each PCI device, including a PCI-PCI bus bridge, has a set of configuration registers located on the device. In order to configure a PCI device, it is necessary to send commands to each register to write various configuration values into that register and, this, in turn, requires an address for each configuration register.

Because the PCI bus system is memory mapped, each configuration register has an address that is determined by the bus and the slot on that bus in which a PCI device containing that register could be plugged. Of course, not all PCI slots will have actual devices plugged into them. However, the configuration register addresses are all predetermined and different for each register. Together, all of the potential configuration register addresses form a configuration address space. Although the PCI configuration address space is in the address space of the computer, reads and writes to these addresses actually read and write registers in the PCI device associated with that address set. This is described in Cepulis at column 4, lines 17-34.

In order to configure PCI devices, each device is first discovered by sequentially proceeding through the configuration address space and checking for a PCI device at

each of the PCI address sets in the configuration address space. Generally, this is done by attempting to read one of the registers, for example, the register that holds the vendor ID. If the vendor ID can be read, then a device exists at that address. If an error occurs then no device is located at that address. Once a device is discovered at a configuration register address, that address is subsequently used to send the configuration commands to the appropriate registers on the device. Thus, configuration commands for each different PCI device will be sent to addresses that are specific to that device (and depend on the bus and slot into which the device is plugged.) These latter addresses will be different for each different device. Different addresses are necessary so that two different devices will not respond to the same configuration command.

The Porterfield patent discloses a method for configuring non-hierarchical ("flat") bus systems as if they were hierarchical. This allows such systems to be configured by operating systems that are expecting to configure hierarchical bus systems. The Porterfield method accomplishes the configuration by making the flat bus system "appear" to the operating system as if it were hierarchical. In particular, the configuration address space is manipulated to make configuration register addresses associated with a second PCI bus appear to correspond to a first slot position on a first PCI bus. Similarly, configuration register addresses associated with a third PCI bus appear to correspond to a second slot position on a first PCI bus. With the configuration address space manipulated in this fashion, all configuration commands can be sent to the first PCI bus. However, configuration commands sent to the first slot position on that bus are in fact associated with the second PCI bus so that the second PCI-PCI bridge responds. Similarly, configuration commands sent to the second slot position on that bus are, in fact, associated with the third PCI bus so that the third PCI-PCI bridge responds.

Although Porterfield discloses configuring flat bus system, it should be noted that the Porterfield configuration process proceeds in the normal fashion for PCI bus systems. Otherwise, an operating system that is expecting a hierarchical bus system could not properly configure the bus system. In particular, each PCI device is still associated with configuration register addresses that are unique to that device. Once a

device has been located by sequentially proceeding through the configuration address space and checking for addresses that return a valid response, further configuration commands are sent to the configuration register addresses that are uniquely associated with that device.

Consequently, while the combination of Cepulis and Porterfield might teach or suggest configuring both flat and hierarchical bus systems, the combination can only teach or suggest sending configuration commands to register addresses that are specific to each device, since both references use this technique.

The present invention is directed to an I^2C or "wired-AND" bus system that uses bus bridges in which each bridge is designed to respond only to configuration commands sent to its assigned bridge ID. In order to configure this system, the configuration software initially sets the bridge IDs of all bridges to the same predetermined bridge ID value. Then, the configuration software sends a configuration command to this predetermined bridge ID value. Normally, since all bridges have the same bridge ID, all bridges on the highest level bus would respond to this command. However, in accordance with the invention, only one bridge on the highest level bus will respond to the configuration command because of the CGF OUT/CFG IN "daisy chain" connections between the bridges at each bus level. Once that one bridge has been configured, the CFG OUT/CFG IN connections cause another bridge on the highest level to respond to the same predetermined bridge ID value. In this manner, by repeatedly sending configuration commands to the same predetermined bridge ID, the entire bus network can be configured.

The claims have been amended to particularly point out this difference. For example, claim 1 has been amended to recite that each bridge responds to configuration commands sent to its bridge ID and in step (a), "initially setting the bridge ID of all bridges to a same common predetermined bridge ID value and walking the bus system to discover the bus topology and the bus bridges that form that topology by repeatedly sending commands and data to the same predetermined bridge ID value" and, in step (b), "assigning a unique bridge ID different from the same predetermined bridge ID value to each discovered bridge (emphasis added). As previously mentioned, the PCI configuration systems disclosed in Cepulis and Porterfield send commands and

data to configuration addresses that are different for each PCI device. Neither reference discloses setting the configuration addresses of all PCI-PCI bus bridges to the same predetermined value. Instead, the configuration addresses of the bus bridges are determined by the bus they are on and their position on that bus or by making it appear that the bridges are located on a bus and position.

Consequently, amended claim 1 patentably distinguishes over the cited combination of the Cepulis and Porterfield references. Claim 18 has been amended in a similar manner to claim 1 and thus, distinguishes over the Cepulis reference in the same manner. Claims 13 and 30 have been amended to conform them to changes in amended claims 1 and 18.

Claims 2-11, 13 and 17 and 19-28, 30 and 34 are dependent on amended claims 1 and 18, respectively, and distinguish over the Cepulis reference in the same manner as amended claims 1 and 18.

Claims 14-15 and 31-32 have been rejected as obvious under 35 U.S.C. §103(a) over Cepulis in view of Porterfield and further in view of U.S. Patent No. 6,260,092 (Story.) The examiner asserts that story discloses all of the claimed limitations except the limitation that bridges on the same level are connected in a daisy chain configuration. However, the examiner claims that story discloses bridges connected in a daisy chain. The examiner concludes that it would have been obvious to combine Cepulis, Porterfield and Story to reduce interconnect signal line count.

First, there is no need to modify the Cepulis and Porterfield combination to prevent more than one bridge from responding to a command issued to the same common address because, in Cepulis/Porterfield, each command is issued to a unique address and only the bridge at that address will respond. Thus, one skilled in the art would not be motivated to seek a modification as disclosed in Story. In addition, while Story discloses ring-connectable bus bridges, it is not directed to bus configuration. Instead, Story is addressed to methods and apparatus for connecting a PCI bus system to a high speed serial link, such as a Fibre Channel. Therefore, Story itself would not suggest a combination with Cepulis and Porterfield. Further, even if Cepulis, Porterfield and Story were combined as suggested by the examiner, the combination would not teach or suggest the limitations recited in claims 14-15 and 31-32. For example, claim

14, which is dependent on claim 13, recites that all bridges on the same hierarchical level are connected in a daisy chain so that only one bridge at a time responds to the predetermined bridge ID value. In Story, the bus bridges are connected in a daisy chain, but not so that only one bridge responds to an address value. Rather the bridges are connected in a daisy chain that passes signals from one bridge to another until the bridge to which the signals are addressed responds. Thus, the combination of Story with Cepulis and Porterfield cannot teach or suggest this limitation because none of the references discloses or suggests it. Claim 15 further recites that the bridge ID must be changes in one bridge before another bridge can respond to the predetermined bridge ID. Story does not disclose this type of operation and neither does Cepulis or Porterfield. Thus claims 14 and 15 patentably distinguish over the cited references. Claims 31 and 32, which contain similar limitations also distinguish over the cited references in the same manner.

Claims 16 and 33 have been rejected as obvious under 35 U.S.C. 103(a) over Cepulis in view of Porterfield and further in view of U.S. Patent No. 6,205,147 (Mayo.) The examiner indicates that the Cepulis/Porterfield combination does not disclose a configuration in which two unidirectional bridges are connected in parallel, but Mayo discloses such a combination.

The PCI bus bridges disclosed in both Cepulis and Porterfield are clearly bi-directional, thus one skilled in the art would not be motivated to seek additional references that disclose two unidirectional bridges connected in parallel. Further, Mayo is directed to packet-switched networks rather than the parallel PCI busses disclosed in Cepulis and Porterfield. Thus, one skilled in the art would certainly not look to Mayo for combination with Cepulis/Porterfield. Finally, both claims 16 and 33 recite that the two unidirectional bus bridges are assigned different bridge IDs. Neither Cepulis, Porterfield or Mayo discloses this limitation and, consequently, neither can the combination of Cepulis with Porterfield and Mayo teach or suggest this limitation. Thus, claims 16 and 33 patentably distinguish over the cited references.

In light of the forgoing amendments and remarks, this application is now believed in condition for allowance and a notice of allowance is earnestly solicited. If the examiner has any further questions regarding this amendment, he is invited to call

applicants' attorney at the number listed below. The examiner is hereby authorized to charge any fees or direct any payment under 37 C.F.R. 1.17, 1.16 to Deposit Account number 02-3038.

Respectfully submitted

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